

“Time is Money”

Serial Data & Clock Jitter

Gigamax and Tiri Technologies



Introductions

- Gigamax Technologies Inc. - Eden Prairie, MN
 - Designs, manufactures, and markets leading edge signal integrity analysis solutions focused on jitter and timing analysis tools which are particularly well suited to test the critical performance of Fibre Channel, Gigabit Ethernet, InfiniBand, USB3, PCIe, SATA, CAUI, XAUI, DDR2/3, Clocks and PLL. (Formerly WaveCrest Corporation)
- Tiri Technologies Inc. - San Jose, CA
 - Test Equipment Manufacturer Sales Representative with 18 years in test and measurement as engineer in failure analysis, application engineering, sales and support.



Overview

- Serial data is used everywhere
- Every receiver also uses a clock
- Timing relationship issues between serial data and their clocks can cause errors
- It is becoming more well known that clock problems can cause severe issues with receiver ability to maintain speed
- Our tools help you define and explore this relationship
 - Determine if there is a problem
 - Find out how close to failure your systems are
 - See the details between pass and fail

Why are we here?

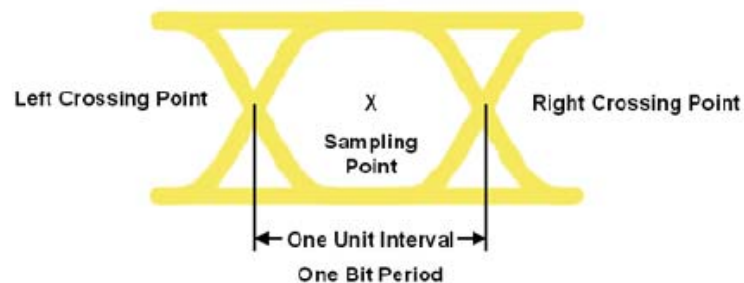
- It is well known that high speed serial data throughput suffers from signal integrity issues
 - Reflections, impedance mismatches, etc.
 - Jitter on data signal
 - Jitter on clocks
 - Jitter on transmitter source clock
 - Jitter on receiver clock
 - Jitter relationship between clock and data
 - Receiver jitter transfer function
- Our tools excel at showing these issues without common measurement errors
 - Eliminate confusion due to equipment variations
 - ScopemaX CTA specifically addresses clock measurement issues
 - Compliance testing does not ensure interoperability
 - Just ensures you have tested the same way others have
 - Your part can pass compliance and not work. **Why?**

What makes us different or unique

- Gigamax Technologies Inc.
 - We measure timing movement. True time domain measurement on differential signals from edge crossing to edge crossing.
 - Accurate repeatable jitter measurements with good separation/isolation of jitter components
 - Ease of use
 - Full documentation of all test results & raw data storage
 - Failure analysis and debug
 - Used for reality check to insure stress impairment jitter settings of other equipment is accurate with good isolation of Rj and Pj.
 - Measures higher frequency jitter that is important in serial data systems.
 - Provides results in time & frequency domain units to compare with datasheets and other instruments.

What makes us complementary

- Clocks & High Speed Serial Data Testing Suite of tools
 - Serial data testing requires multiple test instruments
 - Protocol traffic generators and analyzers
 - Pattern Generators
 - Sampling Oscilloscopes
 - Real Time Oscilloscopes
 - BERTs
 - Stress Impairment jitter generators
 - Compliance boards and fixtures
- Gigamax ScopeMax
 - Is a real time measurement instrument with a sampling oscilloscope to validate or investigate the components of jitter using the memory, display, pc of a real time scope.

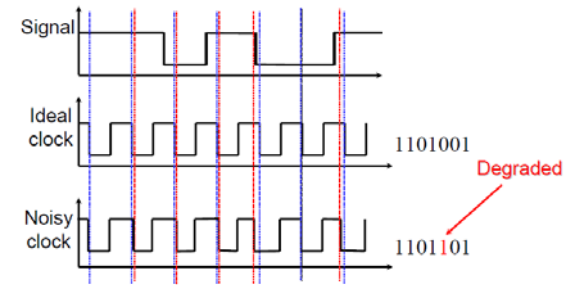


Real Issues resolved by Gigamax

- ORT: Crystal Oscillator lot code variation due to cost reductions by supplier caused different margins producing hard drive electronic system failures.
- Intermittent failures on functional test or in field
- Calibration of jitter for Characterization testing. Isolating the different components of jitter: R_j , P_j
- Debug system level with multiple clock domains
- Long term testing for varying temperature / voltage / environmental ties up expensive equipment. Use strip charts in Scopemax.

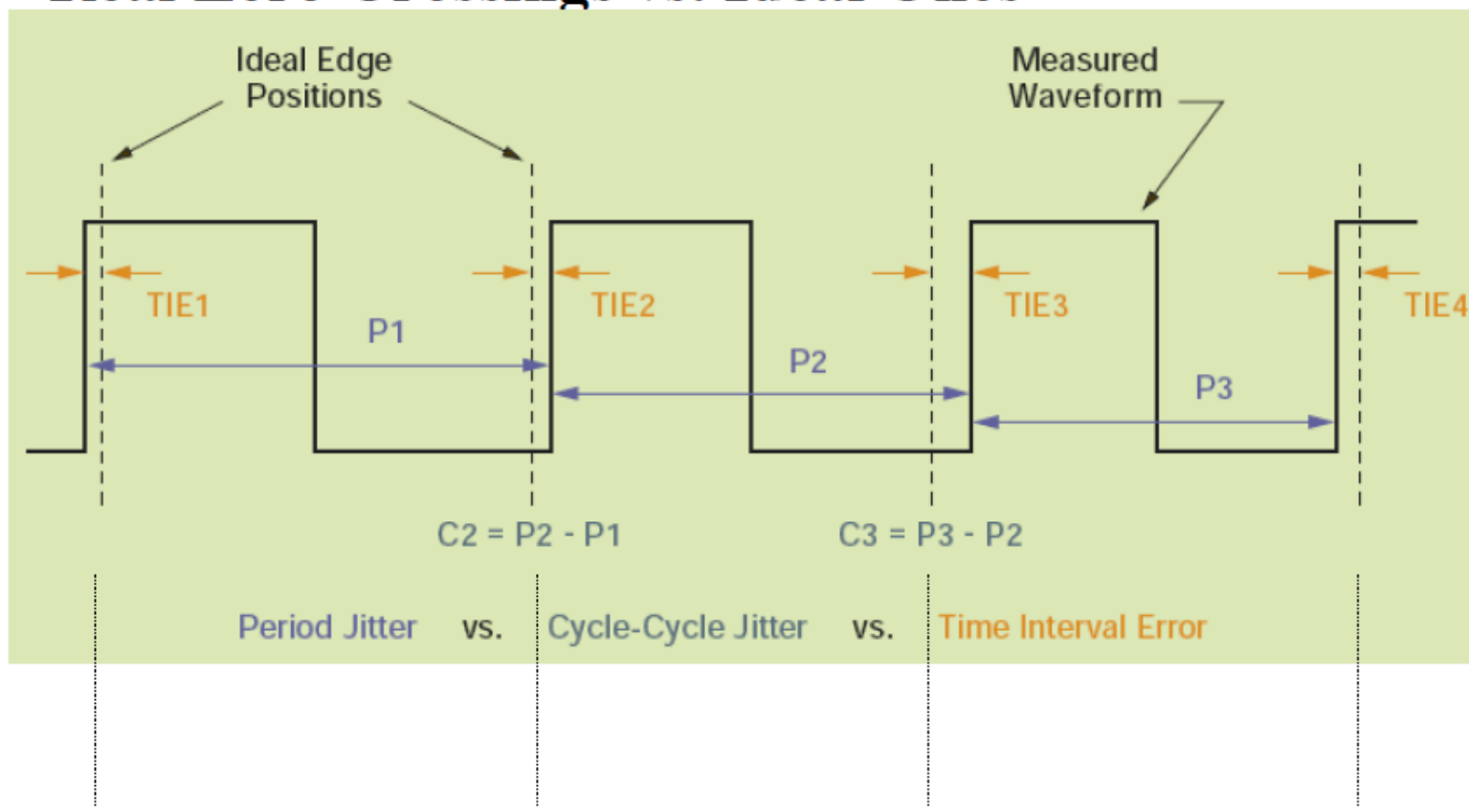
Why measure clock jitter?

- Clocks are vital to downstream parts. Jitter causes transmission errors. BERTs measure errors, but provide little information on them, but jitter does.
- Jitter transfer is how much jitter at the input is transmitted to the output as a function of the jitter frequency.
- A Clock is multiplied up to create serial data
 - $62.5\text{MHz} * 192 = 12\text{GHz}$
 - What happens with the jitter if signal has 192 times more bandwidth?
 - Receiver CDR determines jitter frequencies of concern
 - Pay attention to spurs or PJ frequencies
- Using generic tests or datasheet values may not be good enough
 - Very specific tests may be needed



ScopemaX measures the timing movement

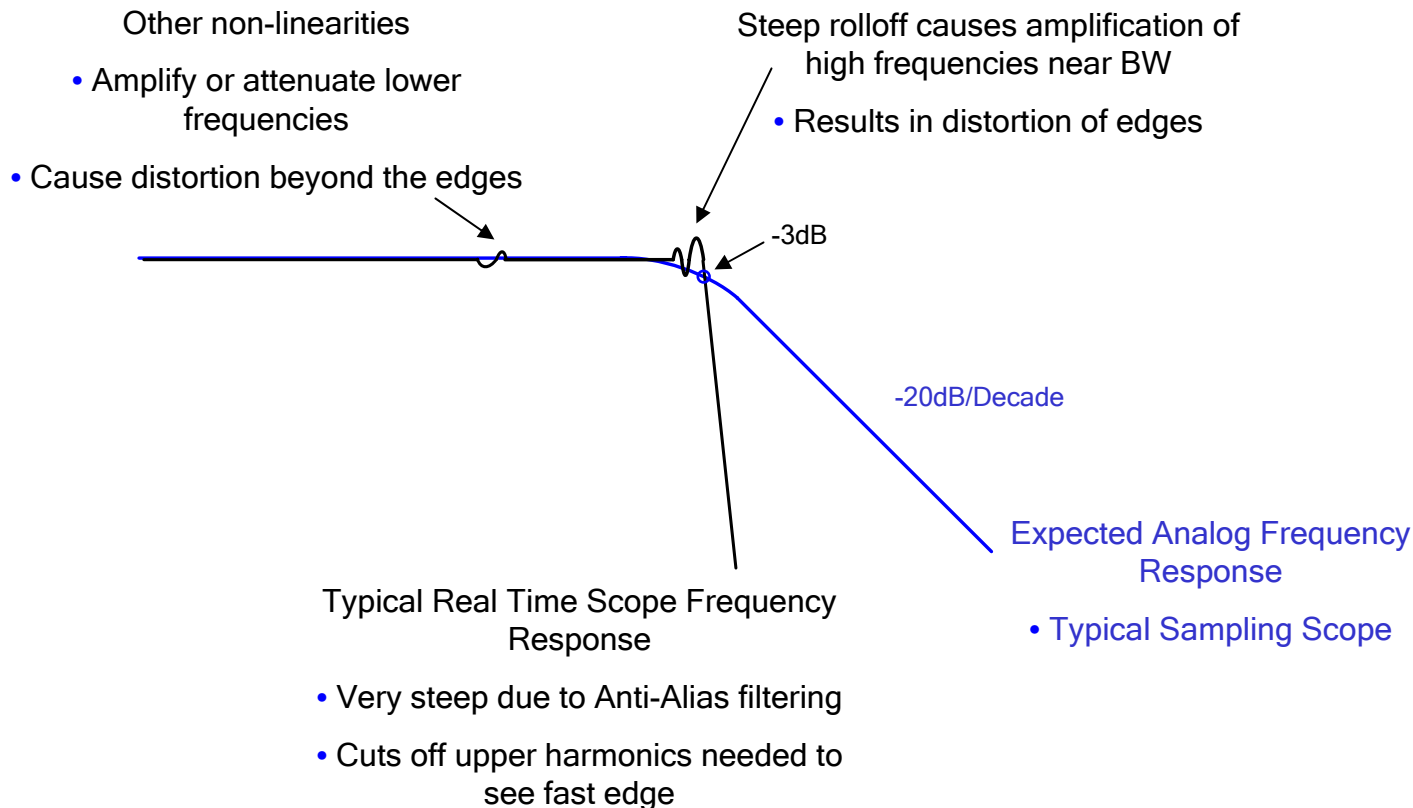
Real Zero Crossings vs. Ideal Ones



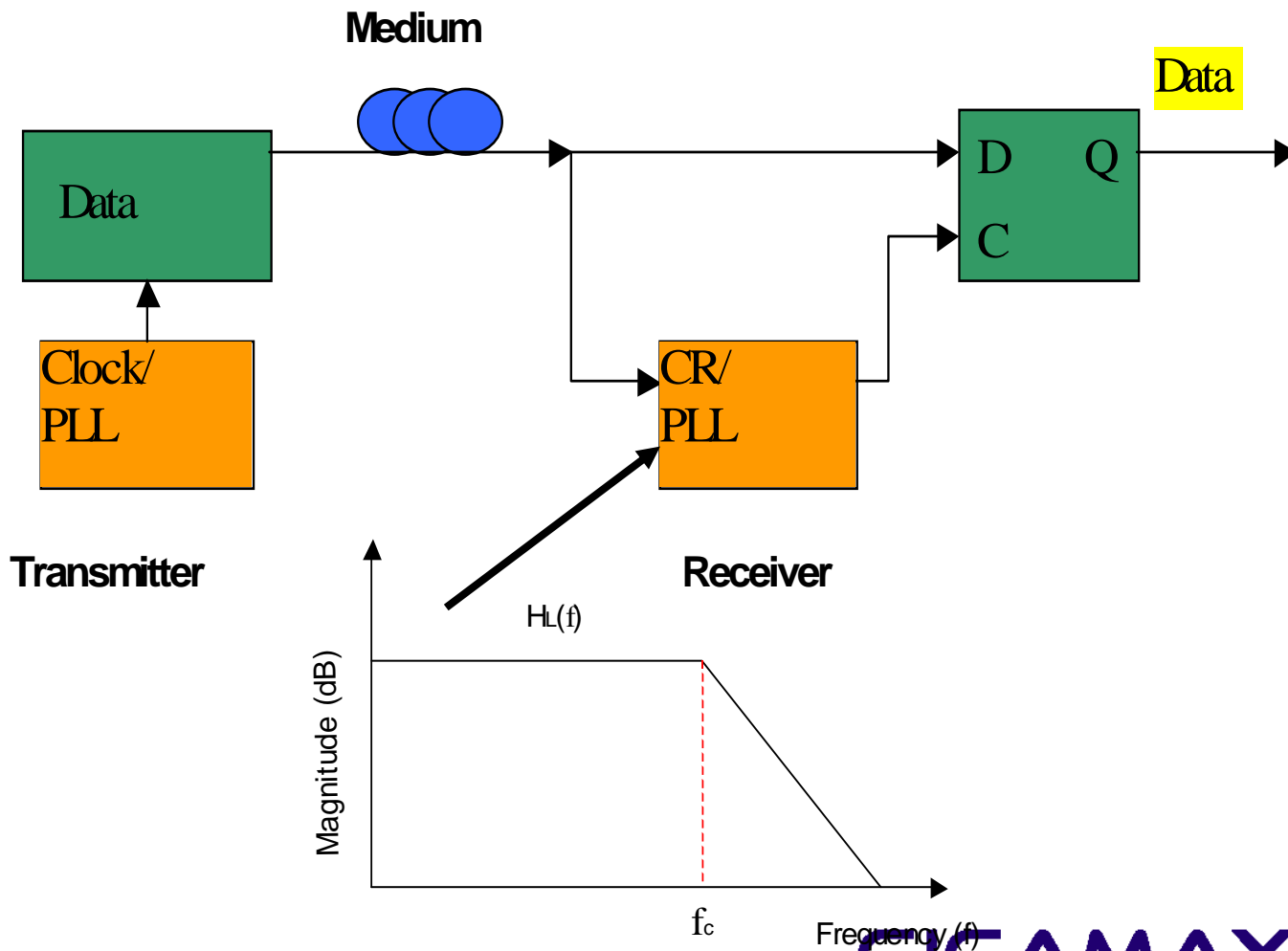
Distortion in all Real Time Oscilloscopes

- No matter what team you play for Agilent, Lecroy, Rohde & Schwarz, Tektronix, or Yokogawa Real Time Scopes suffer from:
 - Front End Amplifier Noise
 - Quantization Noise due to Vertical Gain Setting
 - Digital Front end with anti-aliasing filters with brick wall filter response produces distortion
 - Time Base Jitter
 - Jitter is calculated from the voltage waveform picture with unit to unit variation
 - Interpolation technique varies by scope brand
 - Delta-time inaccuracies increase as measured time increases

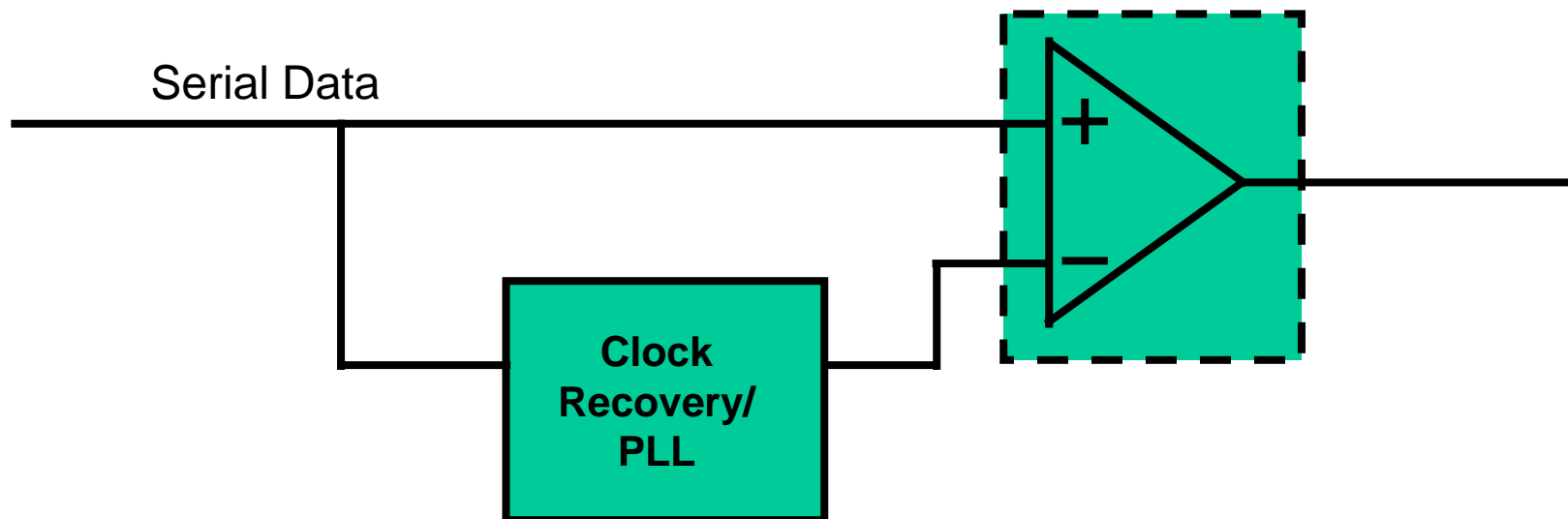
Measurement Equipment: Analog vs. Digital Frequency Response



A Serial Data Communication System



Receiver Jitter Transfer Function



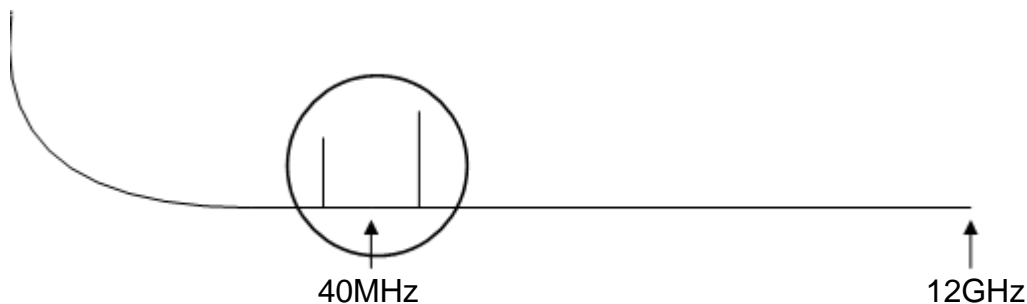
Receiver sees a “Difference” Function

- The difference of the position of the reference clock edge to the data edge

What Is A Receiver Difference Function?

- Jitter is referenced to a recovered bit clock
- Receiver has a jitter transfer function
- “Intrinsic” jitter is not the jitter “seen” by the receiver
- BER of the system should be estimated based on jitter “seen” by the receiver
- Cannot assume a PLL will clean up all jitter
 - Depends on the spectral content of jitter
- Any jitter on the source clock has a potential to cause errors in receiver

Clock jitter measurement question



- Example: 62.5MHz clock phase noise curve
 - With spurs above and below 40MHz limit of phase noise analysis
- Multiplied by 192 to make 12GBs data
 - Very wide bandwidth
- Do the spurs multiply also, resulting in 192 of them? Or do they combine to create one large spur at a very high frequency?

How To Properly Measure These Clocks

1. Use ScopemaX CTA



- Provides all typically needed results in one view
- Detailed graphical results for investigative work
- Very wide jitter measurement band
 - From approx. 1kHz all the way up to frequency of input clock
 - Satisfies receiver difference function measurement requirements

2. Biased Measurements based on instrument and may be difficult to repeat

- Potential to ship bad parts



Important to know

I hope we all realize Time is Money, why not measure time...

We appreciate and respect your time! Thank you.



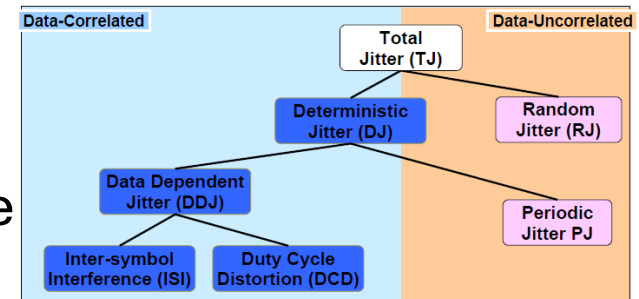
Real example

- 62.5MHz clock has 50MHz periodic jitter component.
 - 50MHz has direct relationship to 12GBs signal
 - Phase noise curve with 40MHz limit did not show spur
 - Two similar but different brand RT scopes did not show this component. They both show DJ as near zero.
 - 50MHz can be confused with DDJ by the scope
 - But, this frequency is a DDJ frequency so it will also cause some DDJ
 - Scopes analysis cancelled out this component completely because it was not seen as PJ
 - 50MHz component was easily seen by ScopemaX and found on spectrum analyzer when shown where to look.

Common Types of Jitter

- Many different jitter terms and definitions

- Clk: Period Jitter, Cycle to Cycle
- Long Term Jitter
- Data: TIE Phase Jitter / Phase Noise
- Time Interval Error (TIE)



- R_j (Random Jitter) random changes on the phase, assumed to be Gaussian distribution, thermal or shot noise, has a multiplicative effect on T_j . $T_j @ 10^{-12} = D_j + 14 * R_j$
- P_j (Periodic Jitter) is a Deterministic component periodic variation in phase. Caused by external coupling, crosstalk, simultaneous switching outputs, power supply noise, counters or registers, PLL comparator feed-through, etc...
- $DCD + ISI$ (Duty Cycle Distortion & Inter-Symbol Interference) is a Deterministic component aka Data Dependent Jitter (DDJ). Bandwidth effects of traces, cables or connectors, saturation, turn-on delay, amp offset, rise & fall times.

CR PLL Frequency Response

“Corner Frequency”

- Frequency response “corner” frequency f_c is determined by clock recovery subsystem
- Many serial data communication standards adopted the “1667” rule, e.g., FC, GBE, SONET
 - $f_c = \text{Databaud}/1667$
- For PCIe v1.1, this corner frequency f_c is 2.5 Gb/s divided by 1667 or 1.5 MHz. For SATA3 6.0Gb/s f_c is 3.6MHz.